LOW POWER GDI FULL SWING FULL ADDER DESIGN FOR AREA AND ENERGY-EFFICIENT DSP SYSTEMS

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Abstract: *In recent years, with increasing demand and the popularity of portable electronic products, the researchers are driven to strive for smaller silicon area, higher speed, longer battery life and enhanced reliability. All these parameters can be achieved by using GDI based full swing full adder at ultra-low-voltage. In most of the digital systems, adders lie in a critical path which influences the overall system performance. Power consumption and speed would be the other two important criteria when it comes to the design of full adders .In this paper a new hybrid 1-bit full adder circuit is designed using 45nm, 90 nm, 180 nm technologies at ultra low voltage of 0.45V, 1V and 1.8V by using tools like Tanner tools and H-Spice .This proposed circuit reports with better performance parameters like low delay, high speed, and lesser power consumption.*

Keywords: Ultra low voltage, GDI, Full swing

1. INTRODUCTION

The Full Adder is the fundamental gate in many arithmetic circuits, such as adders and multipliers. Since these circuits strongly affect the overall speed performance in current digital integrated circuits their speed optimization is crucial in high-performance applications, and typical applications generally require a tradeoff between power consumption and speed [10]. The advances in VLSI technology allow hardware realization of most computing intensive applications such as multimedia processing, DSP, to enhance the speed of operation. The performance of digital circuits can be optimized by proper selection of logic styles. Different logic styles tend to favor the accomplishment of one performance aspect at the expense of others. The logic styles are varied in the method of computing intermediate nodes, the number of transistor count, though they are implementing the same function.

2. CONVENTIONAL FULL ADDER CIRCUITS

2.1 Complementary pass transistor logic:

A CPL gate consists of two NMOS good judgment networks, two small pull-up PMOS transistors for swing restoration, and two output inverters for the complementary output signals. All two-input functions can be implemented with the aid of this fundamental gate structure, which is enormously steeply-priced for simple monotonic gates such as NAND and NOR. The advantages of the CPL fashion are the excellent output using functionality due to the output inverters, and the fast differential stage due to the cross-coupled PMOS pull-up transistors. This differential stage, on the other hand, leads to significantly larger short-circuit currents. Other dangers of CPL are the big range of nodes and excessive wiring overhead due to the dual-rail signals [9].

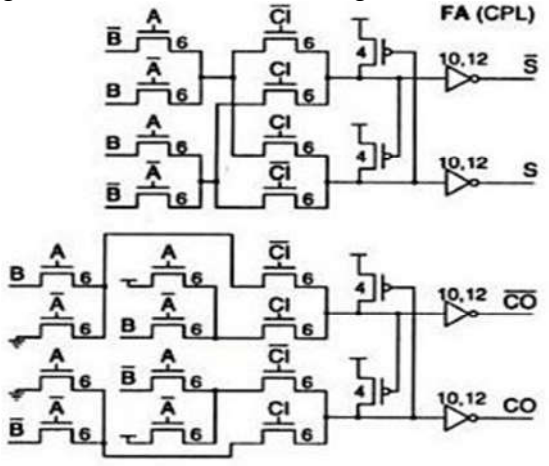

Figure 2.1: Complementary Pass Transistor Logic

2.2 Transmission Gate Logic Full Adder:

Despite of the excessive pace performance of a single TG adder, cascaded TG adders are well regarded to be very sluggish for typical number of cascaded gates, in view that they are equivalent to an RC ladder network. Usually, the lengthen of an RC circuit is decreased by using interrupting the RC chain with repeaters. This thinking can also be applied to chains of Full Adders barring riding capability, such as TG adders, with the aid of interrupting them through a gate having riding capability. In this mixed-topology method to put in force Full Adder chains is analyzed with the aid of thinking about chains of TG adders interrupted via static gates with riding capability to make the most each the high pace achievable and the low energy consumption of the former, as properly as to avoid the velocity degradation related with lengthy chains.

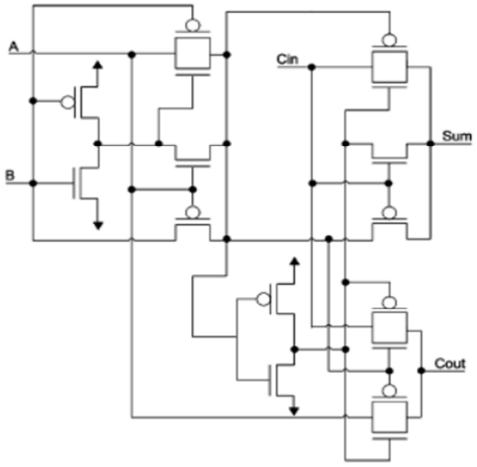

Figure 2.2: Transmission Gate FA

2.3 Gate Diffusion Input:

The GDI full adder employs only 14 transistors as shown in Figure. One XOR/XNOR, two multiplexer's, one Swing Restored Transmission Gate (SRTG), and the different one is Swing Restored Pass Transistor (SRPT) block. The XOR/XNOR block is designed the use of GDI technique. Since the course of the inverters used in the XOR/XNOR blocks has no voltage drop, they are included with widespread V_T devices. Since the GDI MUX-1, multiplexes the output of the XOR (A ⊕ B) and the XNOR (A XNOR B) with a manage enter (Cin) to attain the sum function. The carry output (Cout) is generated by the GDI MUX-2, which multiplexes the inputs Cin and B with manage line from the output of XNOR common sense (A XNOR B). In the GDI design, the full swing is ensured using a SRTG at the output of the sum and SRPT at the carry output (Cout).[19]

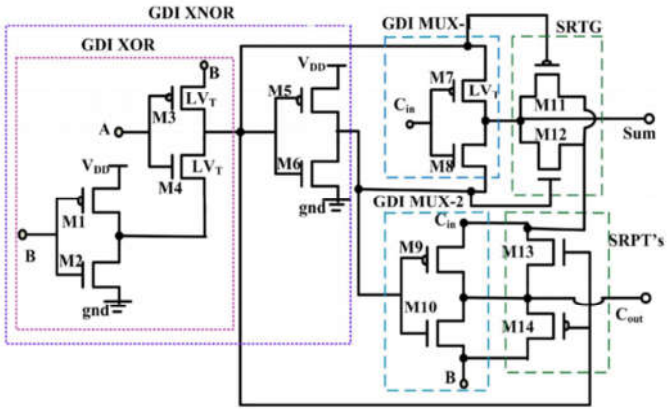

Figure 2.3: 14T GDI full adder design

2.4 GDI XOR FA1 and FA2:

It is very obvious that GDI XNOR FA2 has the minimal Power Delay product. Besides, the GDI XOR FA1 also possesses very small Power Delay product. Hence, the GDI XNOR FA2 is the most effective 10-T based full adder layout while the GDI XOR FA1 is also a preferable choice [20]. But these structures suffer from voltage swing degradation.

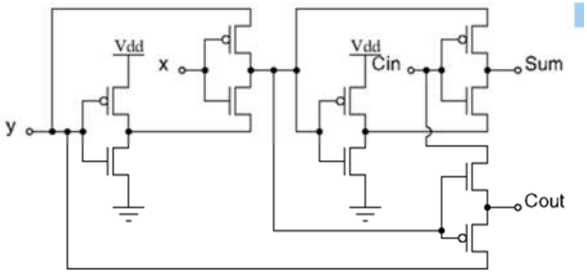

Figure 2.4: GDI XOR FA1

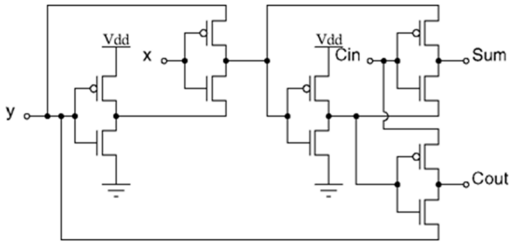

Figure 2.5: GDI XOR FA2

3. PROPOSED MODEL

The proposed format consists of 18 transistors to implement 1-bit full adder as shown in fig. 7. The first feature summation of three inputs A, B, and the elevate out from the previous stage known as Cin implemented via module 1 the use of XNOR-XOR and module2 the usage of XOR. Module 1 has an inverter to generate the feature of 2 transistors Mp1 and Mn1, while Mn2 and Mp2 put into effect A ⊕ B and full swing output performed via swing restoration transistors Mn3 and Mp3. XNOR Function generated by using transistors Mp4 and Mn4 and full swing output done through swing restoration transistors Mn5 and Mp5 rather of an inverter that used in reference [10] to generate XNOR function which consumes greater power, this function power the second module in the circuit. Module two generate the closing output of the summation characteristic as introduced.

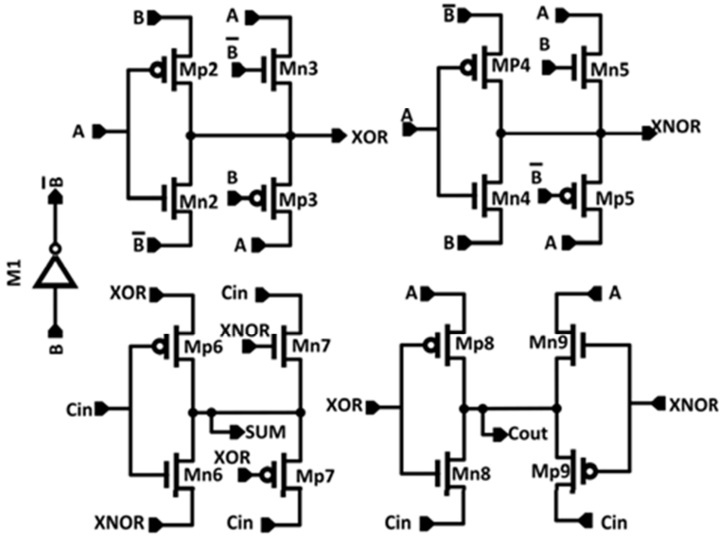

Figure 3.1:GDI Full Swing FA (Proposed Model)

Carry out generated by module 3 which consists of 4 transistors. When (A ⊕ B) equals 1 then Cin passes via Mn9 and Mp8 to carry out, however if it equals 0, enter A passes through Mp9 and Mn8 to carry out to recognize the lift resulting of summation.

4. SIMULATION RESULTS AND PERFORMANCE COMPARISONS

4.1 Schematics and Simulated Waveforms:

Here the different full adder circuits are designed using Tanner Tool whereas simulation waveforms are generated by using H-Spice.

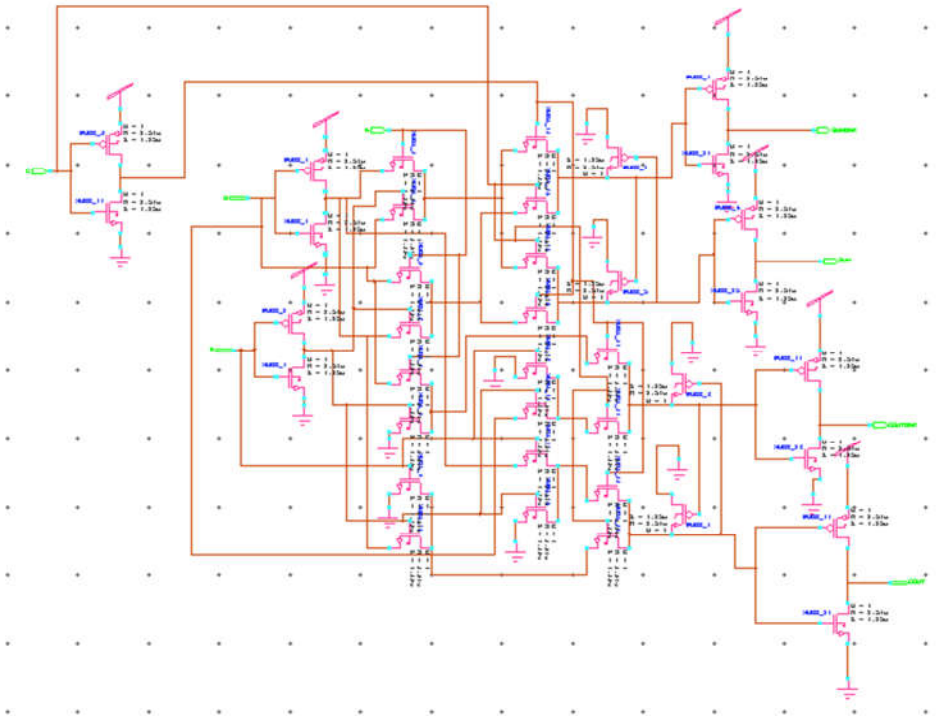

Figure 4.1: Schematic of Complementary Pass Transistor Logic

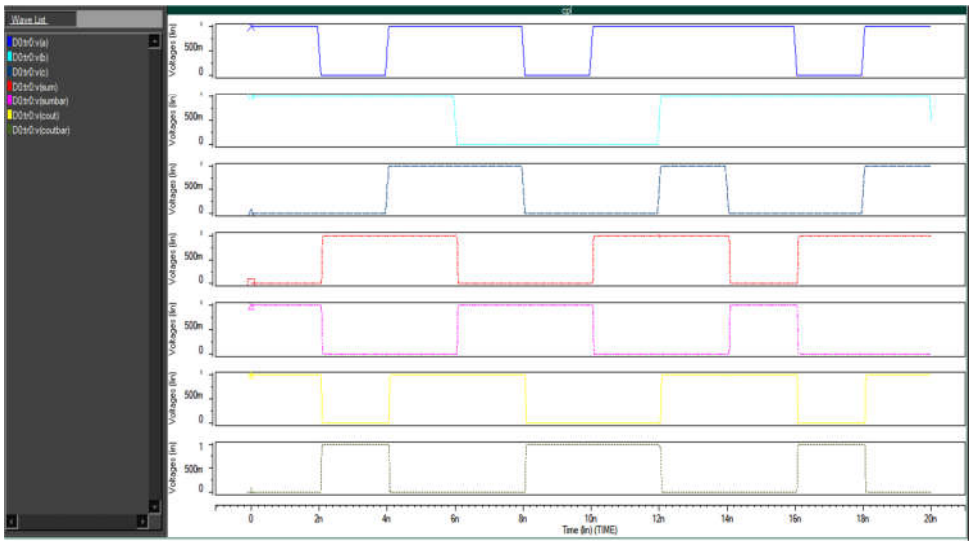

Figure 4.2: Simulated waveform of (CPL)

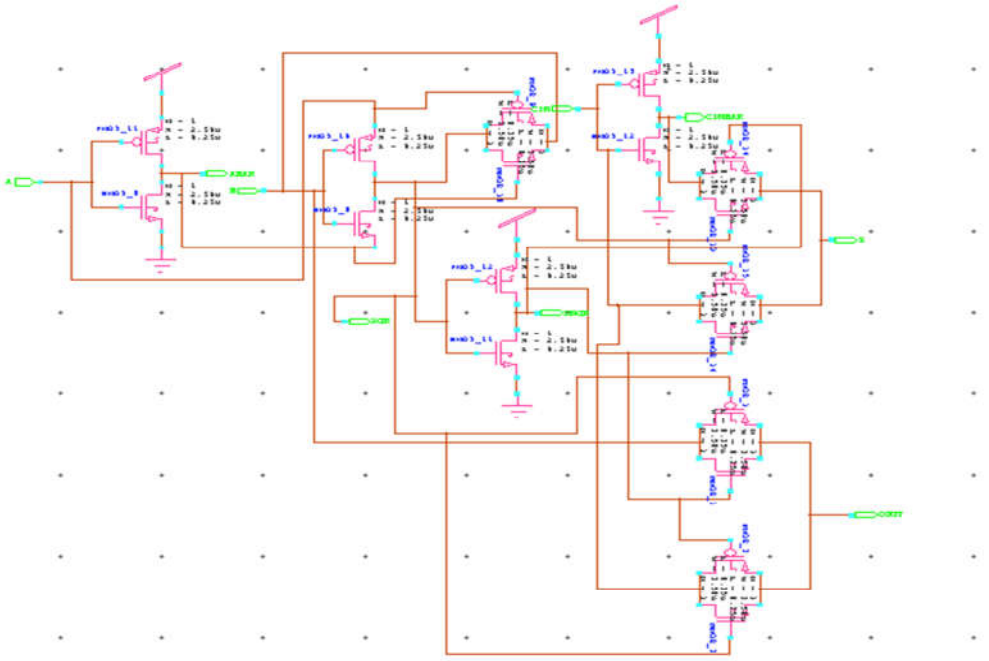

Figure 4.3: Schematic of Transmission Gate Logic

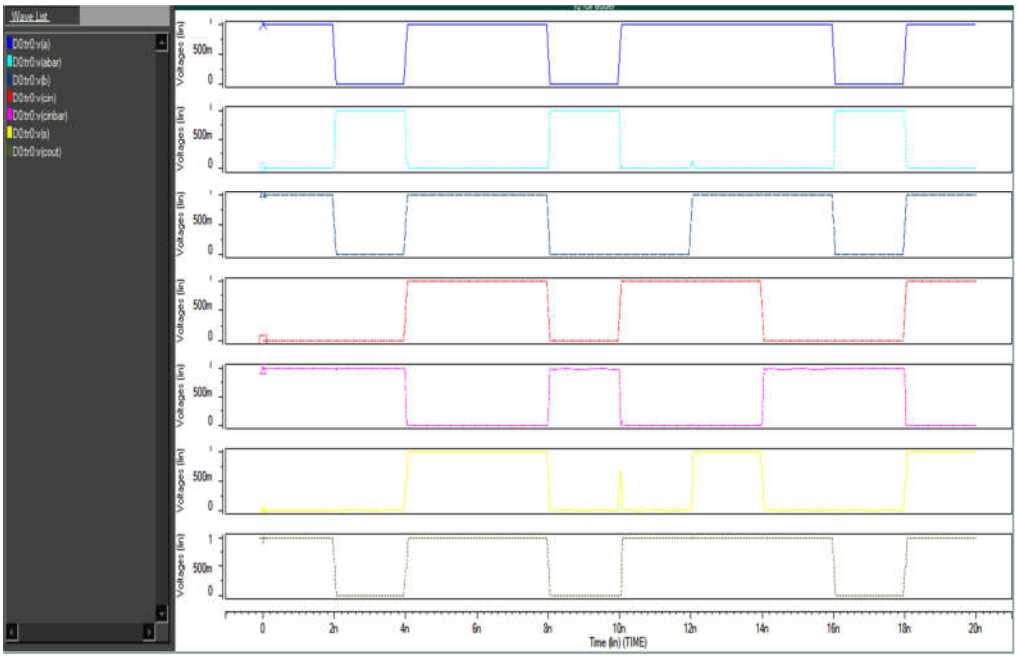

Figure 4.4: Simulated waveform of (TGL)

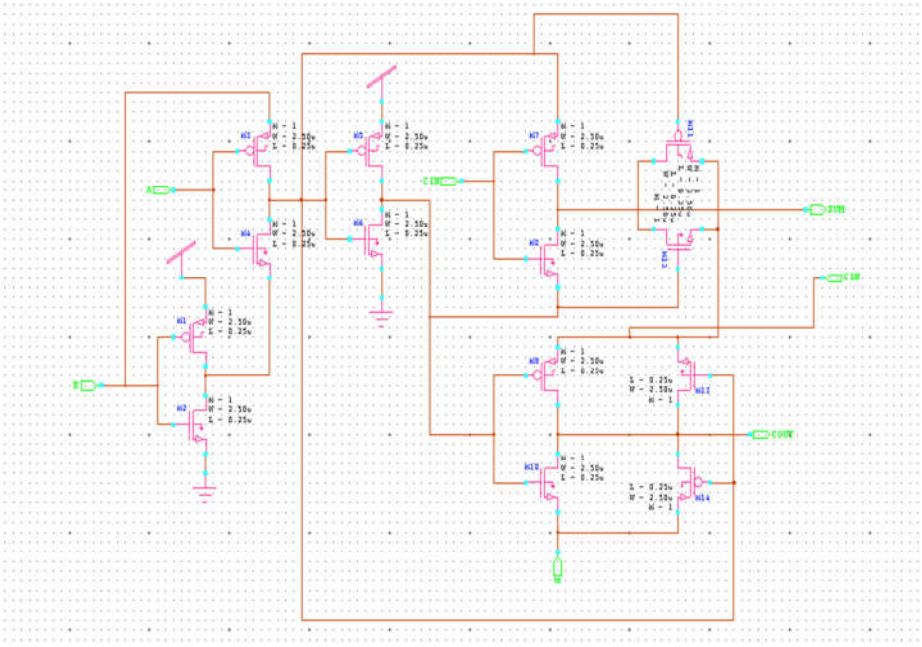

Figure 4.5: Schematic of Gate Diffusion Input FA

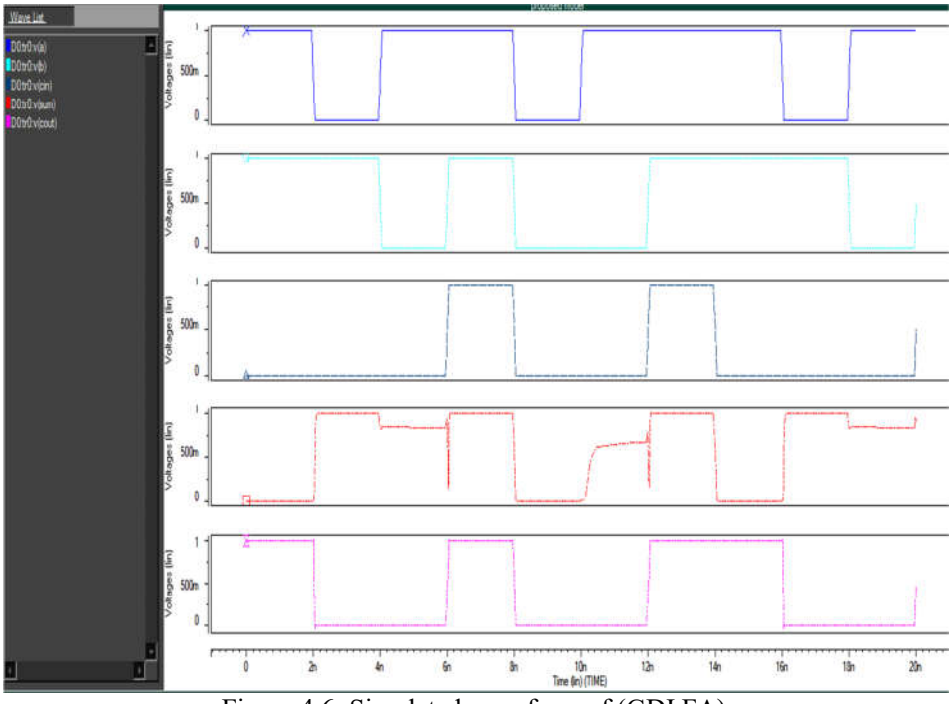

Figure 4.6: Simulated waveform of (GDI FA)

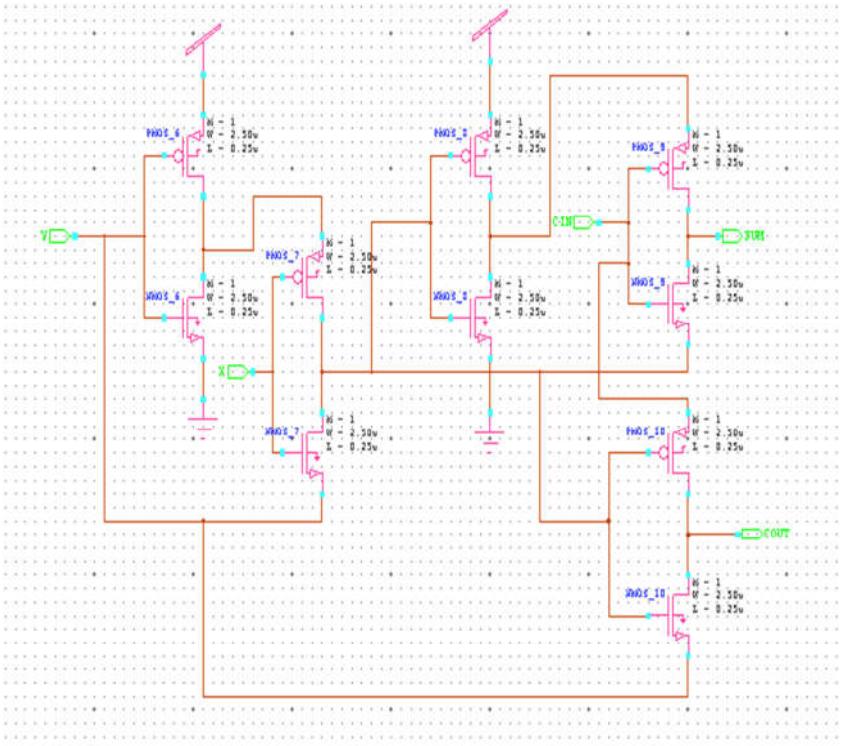

Figure 4.7: Schematic of GDI XOR FA1

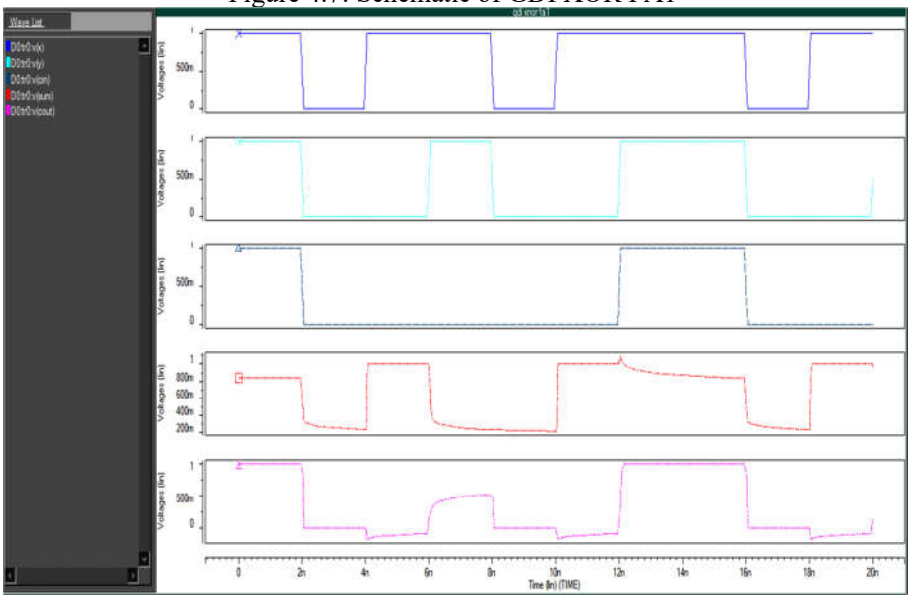

Figure 4.8: Simulated waveform of GDI XOR FA1

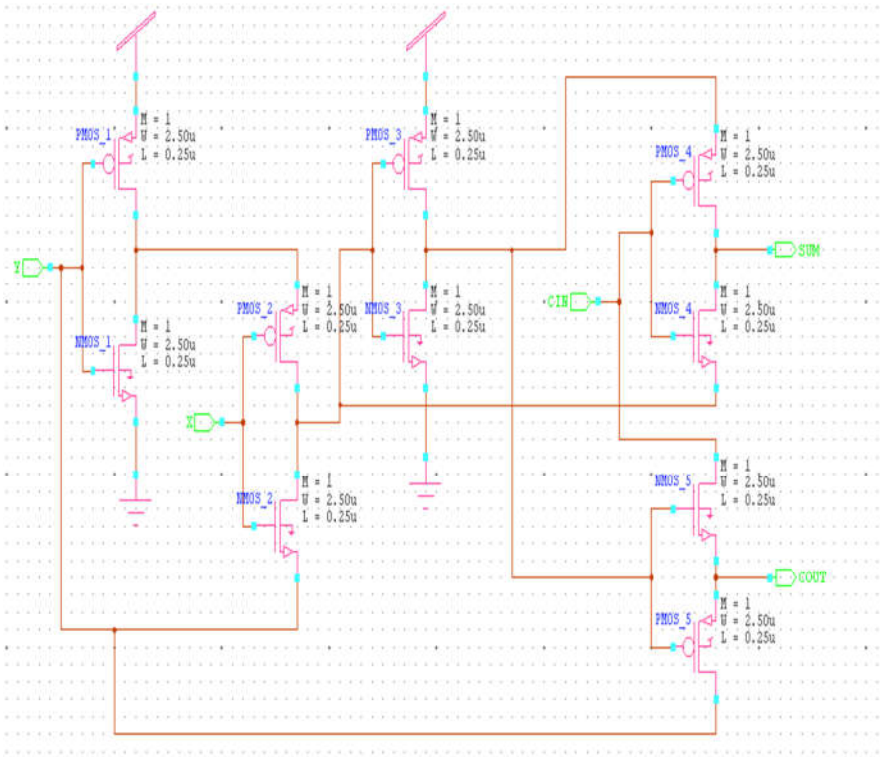

Figure 4.9: Schematic of GDI XOR FA2

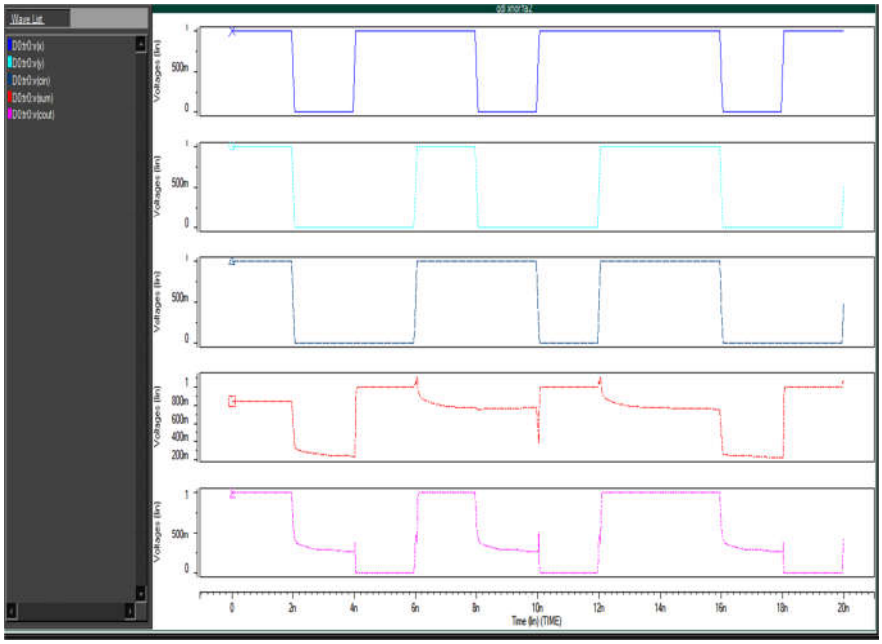

Figure 4.10: Simulated waveform of GDI XOR FA1

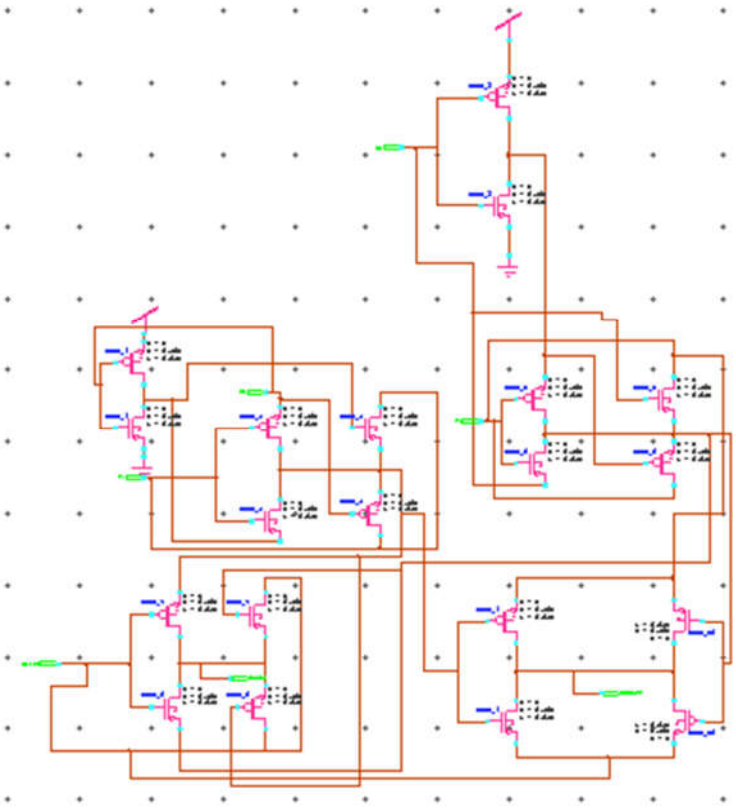

Figure 4.11: Schematic of Proposed GDI Full swing FA

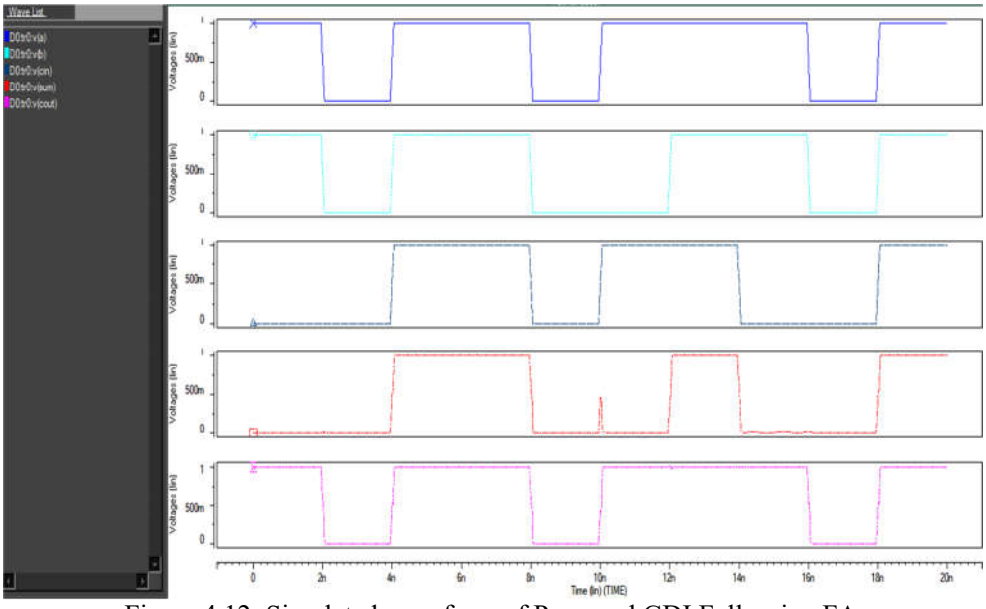

Figure 4.12: Simulated waveform of Proposed GDI Full swing FA

4.2 Performance comparison:

To compare the performances of the proposed Full Adder with the previous works, each circuit was designed using 45nm, 90nm and 180nm PTM technology with VDD=0.45V, 1V and 1.8V respectively, f=500MHz, Temp=27^0C, and simulated with HSPICE.

Comparison of the simulation results for different full adder designs in 45nm, 90nm and 180nm technologies as follows.

Table 4.1: Performance Comparison in 45nm

Designs	Average Power, µW	Delay, ps	Transistor Count	Area, μm^2
Proposed Model	0.11	28.9	20	121.5
Mirror (CMOS)	0.15	87.7	28	170.1
CPL	0.35	114	38	230.85
TGA	1.01	2.51	18	109.35
GDI	0.16	33.7	14	90.72
GDI XOR FA1	0.08	110	10	60.75
GDI XOR FA2	0.06	52.1	10	60.75

Table 4.2: Performance Comparison in 90nm

Designs	Average Power, µW	Delay, ps	Transistor Count	Area, μm^2
Proposed Model	1.08	5.8	20	486
Mirror (CMOS)	7.56	28.6	28	680.4
CPL	4.46	44.2	38	923.4
TGA	1.14	26.8	18	437.4
GDI	3.13	12.7	14	418.5
GDI XOR FA1	3.27	40.3	10	243
GDI XOR FA2	2.55	18.5	10	243

Table 4.3: Performance Comparison in 180nm

Designs	Average Power, µW	Delay, ps	Transistor Count	Area, μm^2
Proposed Model	7.06	1.87	20	1944
Mirror (CMOS)	43.01	35.9	28	2721.6
CPL	30.2	59.6	38	3693.6
TGA	7.70	7.93	18	1749.6
GDI	20.66	2.5	14	831.6
GDI XOR FA1	12.94	48	10	972
GDI XOR FA2	9.48	12.7	10	972

The overall performance parameters power, delay, energy, Energy Delay Product (EDP), and diagram place received from the simulations are compared with the different designs reported in the literature. The simulation effects of the full adders with their transistor be counted and graph vicinity are shown in Table 1. To maintain uniformity in comparisons, the full adder circuits presented in Table 1 are operated with a frequency of 500 MHz and at 27°C temperature.The extend metric plays a key function in estimating the power metric of the circuit while running at ULV, considering that the prolong will increase exponentially with the grant voltage scaling [2].

There will be an exponential roll-off of pace when the circuit operating at ULV, limiting the vary of applications to low or medium frequencies [2].The lengthen is measured for all the input transitions, with the aid of taking the difference between 50% of the input voltage swing and the 50% of the output voltage swing. The CPL diagram occupies more location because of its more transistor count and additionally the complexity of its sketch is high due to the presence of greater metallic traces in realizing the logic.

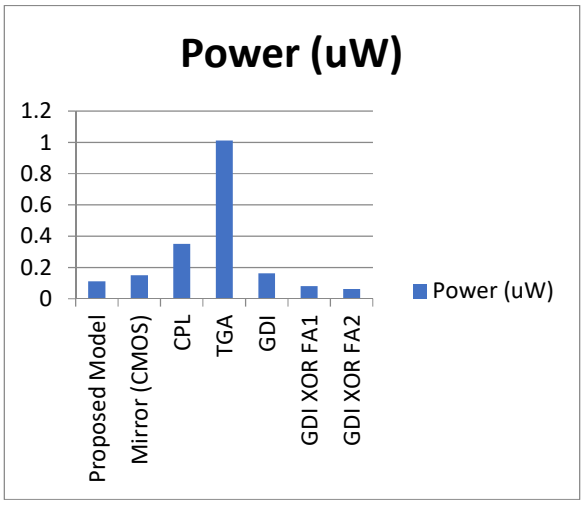

Figure 4.13: Power Comparison in 45nm

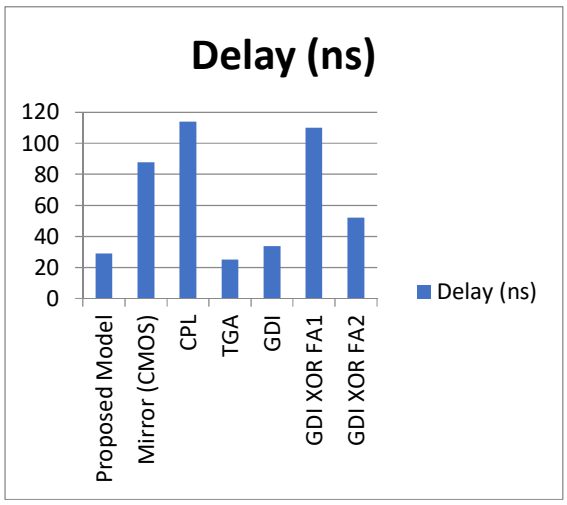

Figure 4.14: Delay Comparison in 45nm

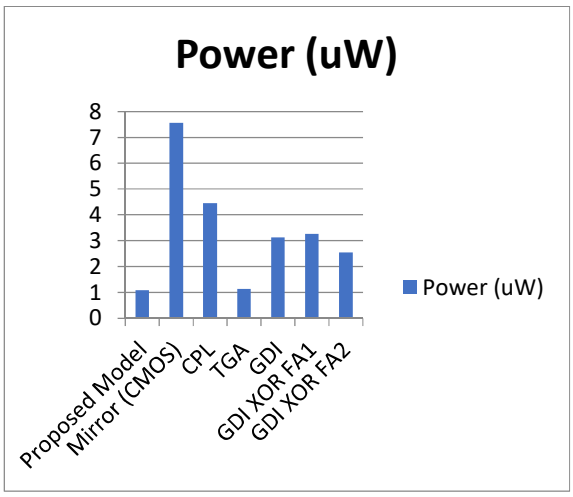

Figure 4.15: Power Comparison in 90nm

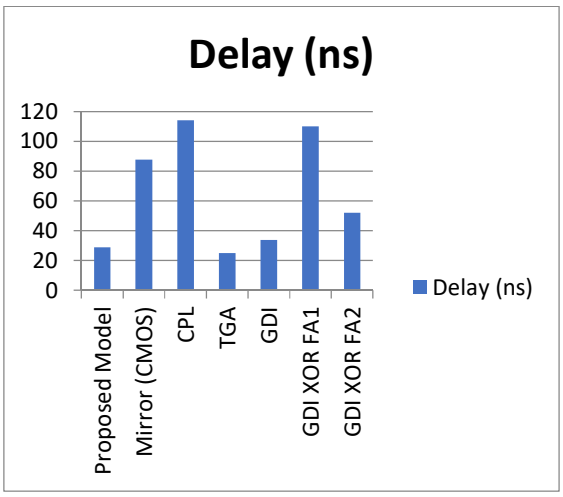

Figure 4.16: Delay Comparison in 180nm

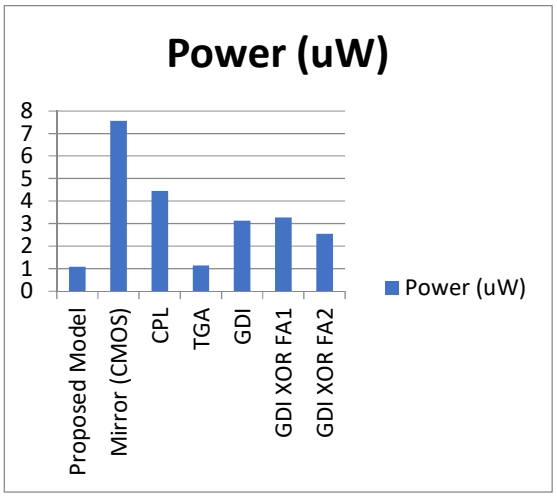

Figure 4.17: Power Comparison in 180nm

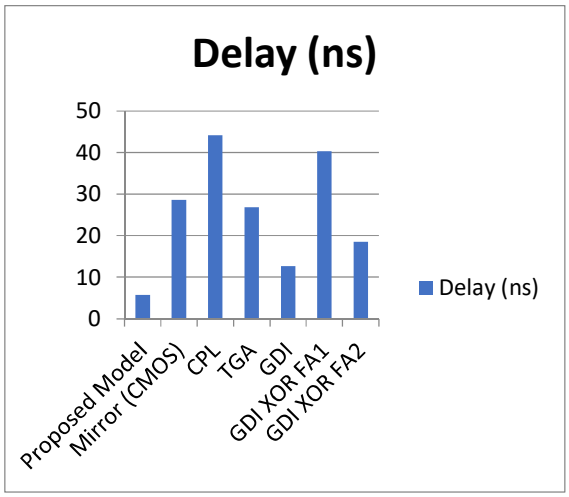

Figure 4.18: Delay Comparison in 180nm

The average power of the proposed model is less when compared to the other GDI techniques. By comparing the proposed model with other designs in different parameters the proposed model is efficient and given the best results.

5. CONCLUSION

Arithmetic sub systems are important part in processors. The current mobile applications and DSP applications need integrated circuits with high speed, less area and low power consumption. In this paper, the Full Adder design circuits for ultra –low-voltage GDI based applications have been presented .The circuits are mainly used for area and energy efficient computing systems. All the designs have been simulated with 45nm, 90nm and 180nm technology using HSPICE and their performance parameters such as average power, delay, area and transistor count are compared. The proposed design shows low power consumption and high speed over the conventional designs. The minimal power consumption of 0.1143μW is achieved by the proposed model compared to CMOS Full Adder, CPL and so on. These results show that power has been drastically reduced in proposed model.

6. REFERENCES

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